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USER'S MANUAL FOR LARGE-SCALE INTEGRATED CIRCUIT LAYOUT CHECK PROGRAM

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16. ABSTRACT

This document describes a computer program that checks for correctness the output of the PRF (Place-Route-Fold) against the net list input to the PRF program. Also included are a description of the computer program and an example computer run.

17. KEY WORDS

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PREFACE

This document is intended to serve as a user's manual for the Large-Scale Integrated (LSI) Circuit Layout Check Program. This program is an outgrowth of Banning Placement-Routing-Folding (PRF) program, and is essentially dealing with the correctness of chip design which is becoming much more complicated as the number of cells in a chip increases. Questions often arise concerning the faultless, digitized data for which a systematic diagnostic procedure becomes a laborious, time consuming manual task. It is this program's responsibility to execute a complete chip design diagnosis which may considerably reduce a circuit designer's burden. And it also stands alone as a diagnosis aid with no intention to substitute any function performed either by PRF or Artwork programs. The purpose of this program is to diagnose the agreement between a circuit designer's specifications and a corresponding computer generated chip design layout, as being documented on the Artwork tape.

Presumably each user should have a fair knowledge about the use of Banning Computer Aided Design for LSI circuits. Should any question arise, a review of the Banning PRF user's manual is recommended. If any additional references are needed, the programmer's manual, check program design documentation and the Banning Standard Cell Engineering Notebook should be consulted.

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I. INTRODUCTION

The Large-Scale Integrated Circuit Check Program is dealing with the correctness of chip design layout generated by the Banning Placement-Routing-Folding (PRF) program. The objective is to verify agreement between a specified circuit design and a corresponding computer generated circuit layout as stored on the Artwork (PRF output) tape. This program produces a complete listing of error messages. Each incorrect situation and physical location of the components involved are given along with the signal and power lines which are being identified and analyzed. No attempt is made to optimize cell interconnections, construct the circuit data set, or perform a final circuit schematic error check. This program checks for incomplete nets, missing pins in an intended net, improper pins in a given net, dead-end lines, and unwanted components and line segments. An effective check scheme was devised for these purposes, based on artwork tape data, user's specifications and the Banning LSI design ground rules.

Both types of LSI circuit design, P-channel and complementary metal-oxide-silicon devices are acceptable to this program. Hence the type of device request parameter must be specified in the first input data card followed by PRF input data deck. Since the deck describing the intended circuit has been assembled prior to a diagnosis run, only one additional card defining the type of device is required to execute this program. Possible mistakes, which might be introduced during preparation of the check program job deck are reduced to a minimum by adopting the same card deck used to execute the PRF program. Inputs to this program comply with the Banning design specifications and its data format.

The basic design of the check scheme is to reconstruct each pin-to-pin signal, power and ground connections from the artwork data (PRF output). Prior to each diagnostic job execution, the first input card is a device type identifier which initiates the data processing routine. All of these input parameters are being processed and the necessary information pertaining to the Banning Standard Cells are then extracted and stored in individual arrays. Information regarding the interchangeable pins of a known cell are obtained from circuit type files, which may be extracted from either card or tape library. Interconnections are to be constructed by selecting a proper component, a tunnel or a metallization segment from the component or line set data which have been read from PRF output tape and properly saved in separate arrays. Each pin's physical location on a given component is computed in accordance with its reference location and orientation, while that pin is being processed.

The tracing routine then arbitrarily selects an appropriate pin to initiate a reconstruction cycle. When it comes to a nodal point, each data array is searched for the intended pin, tunnel and metal segments. If found, they are registered in an array for analysis purposes. After the completion of relevant information gathering at this point, the reconstruction process then takes on the next point moving along one of the collected but untraced branches. The same information gathering procedure is then repeated at each new point until no related pins are left, and each registered branch within the same net has been traced. The routine will then initiate a new reconstruction cycle until the entire pin array is exhausted.

Subsequently, the above collected information is carefully analyzed and the proper registration is taken to record each occurence of incorrect layout. All error situations which have been evaluated are listed under the proper message category. The clock, power and ground buses are also diagnosed to insure their proper layouts.

Figure 1 illustrates the inputs required to drive this program and job flow.

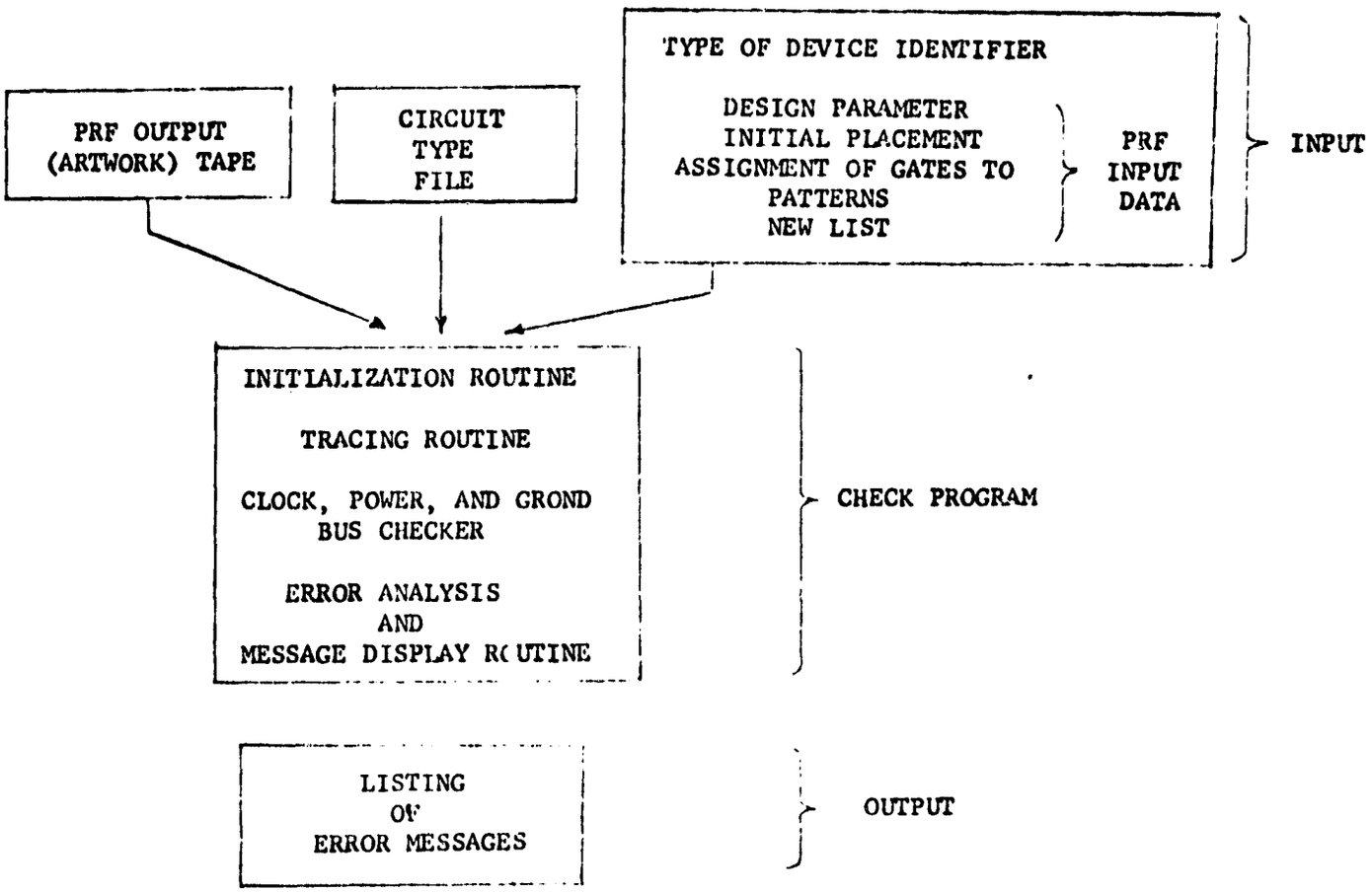

Figure 1. Execution Flow

No automated, computer aided correcting facility has been implemented in this program; the only output is a list of error and warning messages which may be used to direct a mask designer to correct the erroneous situations.

II. JOB SET UP, INPUT DATA AND EXECUTION

The executable check program is stored in a system library tape and available to anyone who would like to diagnose his Artwork file. The program is implemented in the Xerox Sigma 5 system and may be executed with the following set of system control cards:

```
'JOB name, account number
'ASSIGN F:1,(DEVICE,7T),(SN,CTF),(BCD),(IN)
'ASSIGN F:10,(DEVICE,7T),(SN,AWRK),(BCD),(IN)
 ASSIGN F:5,(DEVICE,CRA03),(BCD)
 RUN (LMN,DTMP)
 DATA
                          |
                          |   TYPE OF DEVICE IDENTIFICATION CARD
                          |
                          |   PRF PROGRAM INPUT DATA DECK
                          |
'EOD
'FIN
```

Since all input data used to drive this program are exactly the same as that set used to drive Banning PRF program, no further explanation is needed except some additional mandatories which are stated in the following:

1. First input parameter card is a type of device identifier card. It may either contain "PMOS" for P-channel or "CMOS" complementary device, in the first field of 20A4 input format.

2. Circuit type file may be entered from tape on tape drive unit 1. If an alternate card library is used, it should be included in the input data stream immediately after the circuit type file parameter card.

3. Assignment of GATES TO PATTERN data is entered from the card reader on unit 5, with header and number of pattern cards included.

4. Net list data which provides pin-to-pin signal interconnection information is entered from the card reader on unit 5, with header and number cards included.

In addition to the above inputs, Artwork tape data which contains generated mask layouts is entered from tape drive unit 10. A brief summary of above inputs is given below:

1. TYPE OF DEVICE REQUESTED
2. DESIGN PARAMETER
3. INITIAL PLACEMENT
4. ASSIGNMENT OF GATES TO PATTERN
5. NET LIST
6. ARTWORK INPUT FILE or PRF OUTPUT

III. ILLUSTRATIONS

Two typical diagnostic jobs are shown in figures 2 and 3. One is for P-channel and the other for complementary devices. A command and two parameter cards immediately following the job card are necessary unless the executable module "DTMP" is already residing in the system. All input data must have been assembled previously for the Banning PRF program so that the only additional required input is the designation of the device type. These designations for "PMOS" and "CMOS" are included in each job stream shown after !DATA card.

IV. COMPUTER OUTPUT AND MESSAGE INTERPRETATIONS

A complete listing of messages will be generated after a diagnosis is completed. For convenience in understanding the incorrect layout, the program copies all user's data onto the output listing, together with the listings of warning and error messages. From these two outputs, warning messages may reveal possible error situations, such as circuit type file status, unemployed pins and segments. Error messages indicate incompletion of a net, missing or stray pins of an intended net. Every pin's status is described by one of the error codes stated in the following:

1. U1 signifies that a pin is correctly placed in its designated net on a chip design, according to circuit designer's specifications.

2. U2 means this pin is not placed in its designated net according to the specifications.

3. P1 indicates that the PRF program has placed this pin on a chip design properly and is in agreement with designer's specifications.

4. P1* means that the PRF program places this pin correctly on a chip, but the layout is made by using one of its interchangeable pins. Though this pin may not be the one originally designated by designer, the circuit layout is still functionally considered to be proper.

5. P2 indicates a pin mistakenly connected to or not belonging to the intended net.

Brief error code interpretations are also given on each separate error listing whenever incomplete interconnections occur.

V. ERROR CORRECTIONS AND MANUAL CHANGE PROCEDURE

Diagnostic messages so produced intend to serve only as a guide to the user for whom the actual situations and exact involvement of pins and line segments may easily be located or identified. All errors found may be corrected through manual change procedure as described in the Banning Placement-Routing-Folding User's Manual, NASA Report No. 70-0021.

```
!JOB HUANG,R000(CAD),1
!PCL
COPYALL LTMDIAG
END
!ASSIGN F:1,(DEVICE,9T),(SN,CTF),(BCD),(IN)
!ASSIGN F:5,(DEVICE,CRA03)
!ASSIGN F:10,(DEVICE,7T),(SN,AMRK),(BCD),(IN)
!RUN (LMN,DTMP)
!DATA
CMOS
MSFC C 0061 16 BIT MULTIPLEXER; C. LAWSON
PLACTAPE    1    1
 PARAMETERS
  85    0    3 144    1    118001800    1    0    0    2    3    0   88   32    0   30
 100    0    0    0    0    0    1    0    0    0   82    8   18    6    8    2  09500
  13   14    0    0    0    0  -10    0    0    0   14   18    0    0    0    0    0    0
   0    0    0    0    0    2    1  091009110   60    0    0    0    0    2    0    0
   6    0    0    0    0    0    0   64   12    4  100   40    0    4    8   20   56  140
   0  015209430921093 00   0960092501600 9260    0    0
 ASSIGNMENT OF GATES TO PATTERNS
 117
   11110   21330   31330   41330   51330   61330   71330   81330   91330
  101620  111620  121620  131620  141620  151620  161620  171130  181130
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
 CIRCUIT TYPE FILE
 INITIAL PLACEMENT
   1   86
   2   87
   3   88
   4   89
   5   90
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
 NET LIST
 113
   1    1    2    2    5    3    5    4    5    5    5    6    5    7    5    8    5    9
                5
   1    1    3  100    2
   1    2    2   39    2  117    2
   1    2    3   17    3
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
                .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .  .
!EOD
!FIN
```

Figure 2. An Example of Loading the Check Program Module and a C-MOS Job

```
!JOB HUANG,ROOO(CAD),1
!ASSIGN F:1,(DEVICE,9T),(SN,CTF),(BCD),(IN)
!ASSIGN F:5,(DEVICE,CRA03)
!ASSIGN F:10,(DEVICE,7T),(SN,AMRK),(BCD),(IN)
!RUN (LMN,DTMP)
!DATA
PMOS
PMOS 24 BIT S W G
PLACTAPE   1   1
 PARAMETERS
  75   0   3 109   1   116001600   1   0   0   2   3   0  88  14   0  30
  80   0   0   0   2   075307520   0   0  56   8  18  32   8   3  27030
  13  14   0   6  14  23  37  10  23  32  16  14  14  15   0   0   0   0
   0   0   0   0   0   3   1   060808070  64  68  21   4  32   4   0   0
   5   0   0   0   6   4   0  40  20   0 100  25 135   4  12  14  84 210
   012001200                  0        1600   0   0
 ASSIGNMENT OF GATES TO PATTERNS
  89
   16280   26280   36280   46280   56280   66280   76280   86280   96280
  106280  116280  126280  136280  146280  156280  166280  176280  186280
  196280  206280  216280  226280  236280  246280  254600  264600  274600
          . . . . . .
          . . . . . .
          . . . . . .

 CIRCUIT TYPE FILE
 INITIAL PLACEMENT
  17   1
  18   2
  19   3
  20   4
          . . . . . .
          . . . . . .
          . . . . . .
 NET LIST
  56
   1   1   2  12   4  13   2  24   4  76   2
   1   1   4   2   4   3   4   4   4   5   4   6   4   7   2   8   2   9
           2  10   2  11   2  12   2  88   2
   1   1   3  25   4  26   3  49   2
   1   2   2  11   4  14   2  23   4  77   2
   1   2   3  26   4  27   3  49   3
   1   3   2  10   4  15   2  22   4  78   2
          . . . . . .
          . . . . . .
          . . . . . .

!EOD
!FIN
```

Figure 3. An Example of a P-MOs Job

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